What is claimed is:

1. A method of manufacturing an integrated circuit package, comprising:

providing a substrate comprising:

a first surface,

a second surface opposite said first surface,

a cavity through said substrate between said first and second surfaces, and

a conductive via extending through said substrate and electrically connecting said first surface of said substrate with said second surface of said substrate;

applying a strip to said second surface of said substrate;

mounting a semiconductor die on said strip, at least a portion of said semiconductor die being disposed inside said cavity;

encapsulating in a molding material at least a portion of said first surface of said substrate; and

removing said strip from said substrate.

2. The method of claim 1, said encapsulating further comprising filling said cavity with said molding material, wherein a surface of said semiconductor die is exposed to said strip.

3. The method of claim 2, further comprising attaching a thermal element to said exposed surface of said semiconductor die.

4. The method of claim 3, said attaching said thermal element comprising bonding a thermally conductive adhesive to said thermal element.

5. The method of claim 4, said attaching said thermal element further comprising attaching said thermal element to said second surface of said substrate.

6. The method of claim 1, said mounting said semiconductor die comprising disposing said die in its entirety inside said cavity.

7. The method of claim 3, said thermal element comprising a copper heat slug.

8. The method of claim 1, said substrate further comprising a multi-layer circuit trace.

9. The method of claim 1, further comprising, after said mounting said semiconductor die on said strip, interconnecting said semiconductor die to a first trace embedded in said first surface of said substrate.

10. The method of claim 9, said interconnecting comprising a thermo-sonic wire bonding process.

11. The method of claim 1, said encapsulating comprising a liquid molding process.

12. The method of claim 1, said encapsulating comprising a transfer molding process.

13. The method of claim 1, said encapsulating comprising encapsulating said first surface of said substrate in its entirety.

14. The method of claim 1, further comprising attaching a solder element to a second trace embedded in said second surface of said substrate.

15. The method of claim 1, said applying said strip comprising applying an adhesive material on at least a portion of said strip to said second surface of said substrate.

16. The method of claim 15, said strip comprising a high temperature stable polyimide.

17. The method of claim 15, said mounting said semiconductor die comprising attaching said semiconductor die to said adhesive material on said strip.

18. The method of claim 1, said applying said strip further comprising sealing a portion of said cavity.

19. A method of manufacturing an integrated circuit package, comprising:

providing a substrate comprising:

a first surface,

a second surface opposite said first surface,

a plurality of cavities, each said cavity through said substrate between said first and second surfaces, and

a plurality of conductive vias, each said via extending through said substrate and electrically connecting said first surface of said substrate with said second surface of said substrate;

applying a strip to said second surface of said substrate;

mounting a plurality of semiconductor dies on said strip, at least a portion of each said semiconductor die being disposed inside each said cavity;

encapsulating in a molding material at least a portion of said first surface of said substrate; and

removing said strip from said substrate to expose a surface of each said semiconductor die.

20. The method of claim 19, further comprising singulating said substrate into a plurality of integrated circuit packages.

21. The method of claim 20, said singulating comprising a sawing process.

22. The method of claim 20, said singulating comprising a punching process.

23. An integrated circuit package comprising:

a substrate comprising:

a first surface,

a second surface opposite said first surface,

a cavity through said substrate between said first and second surfaces, and

a conductive via extending through said substrate and electrically connecting said first surface of said substrate with said second surface of said substrate;

a semiconductor die electrically coupled with said conductive via, at least a portion of said semiconductor die being disposed inside said cavity of said substrate;

an encapsulant material encapsulating a portion of said semiconductor die such that at least a portion of a surface of said semiconductor die is exposed.

24. The integrated circuit package of claim 23, further comprising a conductive member adapted for attachment of said integrated circuit package to an external device.

25. The integrated circuit package of claim 24, said conductive member attached to said second surface of said substrate.

26. The integrated circuit package of claim 23, further comprising at least one wire electrically coupling said semiconductor die with said conductive via.

27. The integrated circuit package of claim 23, at least a portion of said first surface of said substrate being adapted for coupling said integrated circuit package with a second integrated circuit package.

28. The integrated circuit package of claim 23, said substrate further comprising a multi-layer trace embedded therein.

29. An integrated circuit package assembly comprising the integrated circuit package of claim 23 attached to at least one other integrated circuit package.

30. The integrated circuit package assembly of claim 29, wherein one of said integrated circuit packages is stacked on top of at least one of the other of said integrated circuit packages.

31. The integrated circuit package assembly of claim 29, further comprising a heat slug thermally coupled with at least one of said integrated circuit packages.

32. The integrated circuit package of claim 23, said package having a thickness dimension of about one millimeter.

33. The integrated circuit package of claim 32, said package having a width dimension of about seven millimeters.

34. The integrated circuit package of claim 23, said substrate being substantially planar and said semiconductor die being aligned in a plane with said substrate.

35. The integrated circuit package of claim 23, said integrated circuit package being a land grid array.

36. The integrated circuit package of claim 23 said integrated circuit package being a ball grid array.

37. The integrated circuit package of claim 23, said encapsulant material comprising an epoxy.

38. The integrated circuit package of claim 23, further comprising a ring-like trace embedded in said substrate.